### Features:

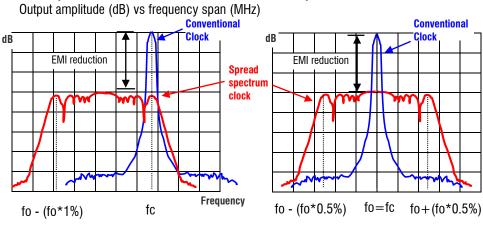
- Lead time: 10 days.
- Reduces system level (both fundamental and harmonic) electromagnetic interference (EMI) by approx. 20 dB
- Drop-in replacement for conventional crystal oscillators, no need to re-spin board layout
- Center or down spread. 6 modulation percentages to choose from for each type
- Operates with a +2.5V or +3.3V supply voltage
- 3.2x5.0 mm or 5.0 x 7.0mm hermetically sealed ceramic package
- Cycle-to-cycle jitter: 100 pS max.
- Compliant to 2011/65 EU RoHS 2 Directive

### **Applications:**

- Printers; Multiple function printers (MPCs)
- Digital copiers; PDAs
- Networking; LAN / WAN; routers
- Storage systems (CD-ROM, VCD, DVD & HDD)
- Scanner; modems; projectors
- Hand-held ID readers

## Modulation Types

#### Down spread:



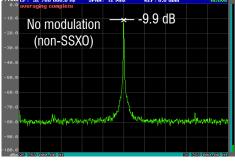
**Center spread :** 

Embedded systems

- Automotive; GPS navigation systems
- LCD PC Monitors / LCD TVs
- ADSL: PCMCIA
- Digital cameras
- Medical equipment and devices

Spread Spectrum Crystal Oscillator (SSXO): Unlike the conventional clock, the mode energy of a spread spectrum clock is spread (distributed) over a wider bandwidth between two pre-defined frequency boundaries by the frequency modulation technique. The modulation carrier frequency is in the KHz range which makes the modulation process transparent to the oscillator frequency. This controlled modulation process can be on all of one side of the nominal frequency (down spread), which is preferred if system overclocking is a concern, or 50% up and 50% down (center spread).

42 MHz non-SSXO vs SSXO at Center Spread 0.25%: 12 MHz 8.0 dBm CENTER FREQ: ( SPAN: 12 MHz REF: 0.0 dBm





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QHM572



MERCURY

Since 1973





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## <u>General Specifications</u>: at Ta=+25°C, C<sub>L</sub>=15 pF

Product Family	quick-turn de	liverv					
	QHM572: Packa		(7.0 x	1.4 mm			
Product Series	QHM53: Packag						
Frequency Range	V <sub>DD</sub> =2.5V: 1 ∼						
	V <sub>DD</sub> =3.3V: 1 ~			• •			
		Spread			r Spread	Total Spread %	
	Spread % -0.25%	Ordering of D0.25		<b>Spread %</b> ±0.125	Ordering code CO.125	0.25%	
Available Spread Type and	-0.25%	D0.23		±0.125	C0.25	0.5%	
Spread Percentage for ordering	-1%	D0.0		±0.20	C0.5	1%	
-F	-2%	D2		±1.0	C1	2%	
	-3%	D3		±1.5	C1.5	3%	
	-4%	D4		±2.0	C2	4%	
EMI Reduction, system level	20 dB typical. Fo	or fundament	tal and	harmonic freque	ncies		
Modulation Carrier Frequency (Dither rate)	31 ~ 40 KHz ty	pical. Freque	ncy de	pendent. Call for	details.		
Output Logic	CMOS Square W	CMOS Square Wave					
Frequency Stability	±50 ppm over ·	$\pm 50$ ppm over -40°C to $+85$ °C; exclude modulation.					
Input Voltage (V <sub>DD</sub> )	$V_{DD} = +2.5V$ or	<sup>-</sup> +3.3V D.C.					
Load	15 pF max.	15 pF max.					
Supply Current; Loaded	15 mA typical, 3	15 mA typical, 3.3V, 15 pF load, 26 MHz					
Output Voltage "High"; "1"	V <sub>DD</sub> - 0.4V min.	$V_{\text{DD}}$ - 0.4V min. $I_{\text{OH}}$ = -4 mA					
Output Voltage "Low"; "0"	0.4 V ma., I <sub>OL</sub> =	: 4 mA					
Output Current	8 mA min						
Output Rise Time	2.0 n sec. typica	==					
Output Fall Time	1.7 n sec. typica		→ 10	% $V_{ m DD}$ , 15 pF lo	ad		
Start-up Time	2 ms typical; 5 r	ms max.					
Duty Cycle	50%±5%. ( C <sub>L</sub> =	=15 pF; at 50	0% <u>V</u> dd	)			
Output Impedance	30 Ω typical.						
Cycle-to-cycle Jitter	100 ps max., 3.	3V					
Aging	±3 ppm per yea	ar max.; Ta=					
Pin 1 Function, Power-down control	When taken LOV			<b>``</b>	cillator, counters an bedance output. Cur	d all other active) rent is 10 $\mu$ A typical.	
	When taken HIG	H or float	Outpu	t			

## Absolute Maximum Ratings

Power Supply Voltage V <sub>DD</sub>	-0.5 V min; +7.0V max.
Input Voltage Range	-0.5V min.; $V_{DD}$ + 0.5V max.
Output Voltage Range	-0.5V min.; $V_{DD}$ + 0.5V max.

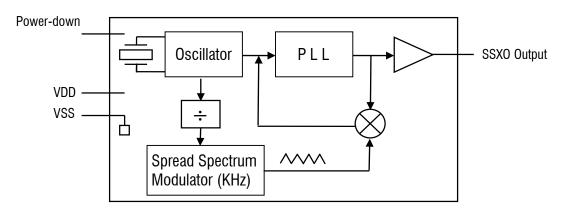
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## **Environmental Performance Specifications**

RoHS Status	RoHS compliant, Pb (lead) free in accordance with EU Directive 2002/95/EC 6/6 (2002/95/EC) and WEEE (2002/96/EC)	
Moisture Sensitivity Level	Level 1 (infinite) according to IPC/JEDEC J-STD-020D.1	
Second Level Interconnect	e4	
Storage temp. range	-55°C to +125°C	
Humidity	85% RH, 85°C, 48 hours	
Fine Leak / Gross Leak	MIL-Std-883, method 1014, condition A / MIL-Std-883, method 1014, condition C	
Solderability	IL-STD-202F method 208E	
Reflow	260°C for 10 sec. 2X.	
Vibration	MIL-STD-202F method 204, 35G, 50 to 2000 Hz	
Shock	MIL-STD-202F method 213B, test condi. E, 1000GG 1/2 sine wave	
Resistance to Solvent	MIL-STD-202, method 215	
Temperature Cycling	MIL-STD-883, method 1010	
ESD Rating	>2000 V (per MIL-STD-883, method 3015)	
Pad Surface Finish	Gold (0.3~1.0 $\mu$ m) over nickel (1.27 ~ 8.89 $\mu$ m)	

#### Block Diagram



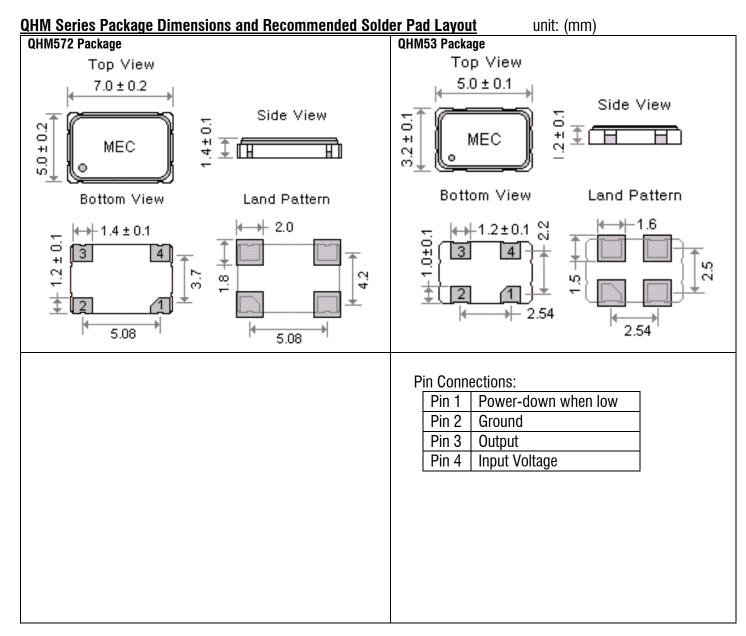
## Part Number Format and Example:

#### Example: 25QHM53D2-66.000

25		QHM			53	D2			—	66.000	
Input \	/oltage	QUIN		Package Code		Package Code Spread Type and Spread %			Frequency	in MHz	
Inpu	t Voltage			Pacl	kage Code	Spre	ead Ty	/pe and	Spre	ad %	
25	2.5 V V	DD	53	3.2	x5.0x1.2 mm	Down Spr	ead	From	D0.25	5 to D4	
3	3.3 V V	DD	572	5.0	x7.0x1.4 mm	Center Sp	read	From	CO.12	25 to C2	

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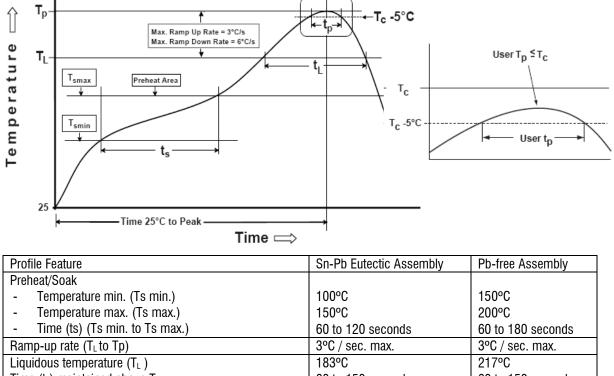




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## Recommended Solder Reflow Profile (per\_IPC/JEDEC J-STD-020D.1)



Time $(t_L)$ maintained above $T_L$	60 to 150 seconds	60 to 150 seconds
Peak package body temperature (Tp)	235°C	260°C
Time (Tp) within 5°C of the classification temperature Tc	10 to 30 seconds	20 to 40 seconds
Ramp-down rate (Tp to T <sub>L</sub> )	6°C / second max.	6°C / second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.

All temperatures refer to topside of the package, measured on the package body surface.

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